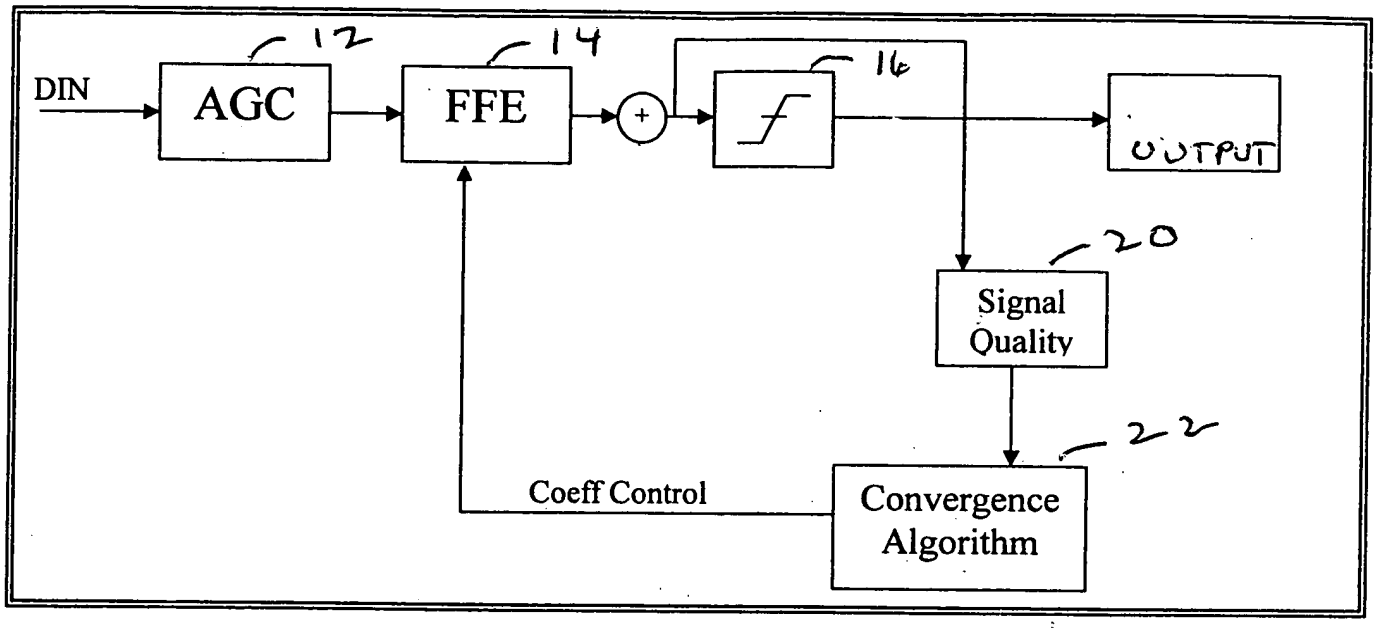
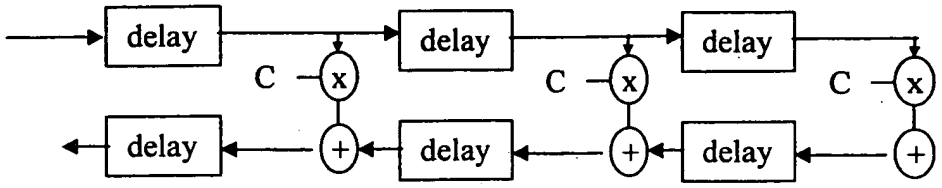
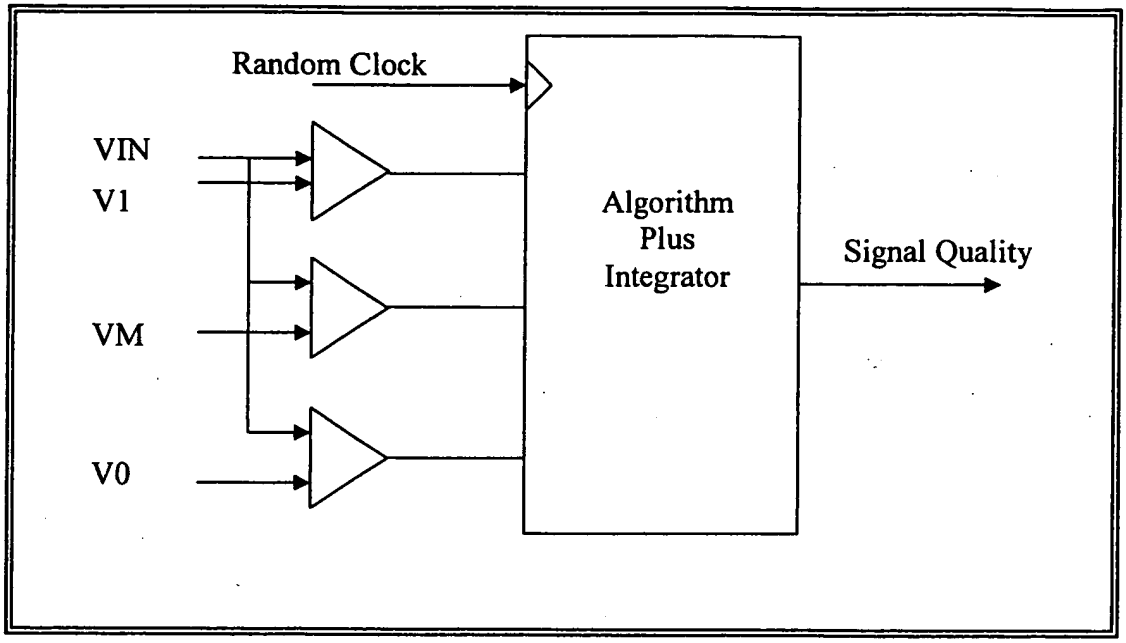

DIN
AGC
12
FFE
14
16
OUTPUT
20
Signal Quality
22
Coeff Control
Convergence Algorithm
10

FIGURE 1



14

FIGURE 2


Random Clock
VIN
V1
VM
V0
Algorithm
Plus
Integrator
Signal Quality

20

FIGURE 3